PCT

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : **H04L 12/40**	**A1**	(11) International Publication Number: **WO 96/37984** (43) International Publication Date: 28 November 1996 (28.11.96)

(54) Title: A DIGITAL DATA BUS SYSTEM INCLUDING ARBITRATION

(57) Abstract

A data bus system is disclosed, including a plurality of nodes coupled together by a daisy chain bus. Each node includes a first and a second bus connection, each having a first and second bidirectional terminal. An arbitration logic is coupled between the first and second bus connection. The node operates in an arbitration mode, during an arbitration time interval, in which the first bidirectional terminal in the first bus connection, and the second bidirectional terminal in the second bus connection are configured to be input terminals, and the second bidirectional terminal in the first bus connection and the first bidirectional terminal in the second bus connection are configured to be output terminals. Then the node operates in a bus access mode in which the first and second bidirectional terminals in the respective first and second bus connections, are both configured to be one of input and output terminals.

1

A DIGITAL DATA BUS SYSTEM INCLUDING ARBITRATION

5
The present invention relates to a data bus system including an improved arbitration scheme for resolving conflicting transmissions from different nodes on the data bus. In digital data bus systems, such as current daisy chain type bus systems, there are two bidirectional signal

10 paths on each data path. More specifically, each data port or node has a bidirectional data line and some form of bidirectional strobe or clock signal line. In such a system, it is possible for two or more nodes to attempt to use the bus simultaneously. In such a situation, such nodes are said to be in contention. Because only one node may use the bus at a

15 time, when two or more nodes are in contention, a decision must be made of which of the nodes is to be allowed to use the bus, a process known as arbitration. Typically, in these systems, the arbitration for control of the bus is initiated by detecting the conflict of the output drivers of the nodes in contention. If two nodes are in contention, the possible states of the

20 bus are:

High	if both nodes are driving high
Low	if both nodes are driving low
Middle	if one node is high and the other is low.

To detect the state of the bus line, three analog level sensors are required. In addition, some form of processing is required after the

25 arbitration is complete to define the direction of the signal transmission for those nodes on the bus between the winning node to the destination node. Multiple level sensors and subsequent processing add cost and complexity to the system.

Fig. 1 is a block diagram illustrating a typical known daisy

30 chain bus system. In Fig. 1, a network of five nodes, A, B, C, D, and E, are connected in a daisy chain bus for interchange of data. Each of the nodes has two connection points, a first connecting to the node on its left (if

2

there is one) and a second connecting to the node on its right (if there is
one). In the illustrated embodiment, each connection point contains two
signal lines (and possibly more). A first signal line carries bidirectional
serial data, and a second signal line carries a bidirectional strobe or clock
5 signal in synchronism with the serial data. The clock signal line is
illustrated as the top-most signal line, and the data signal line is
illustrated as the bottom-most signal line in Fig. 1. In a daisy chain data
bus as illustrated in Fig. 1, the data and clock signal lines are generally
bidirectional and the direction of the clock and data signal lines is
10 switched together. That is, the data and strobe lines always transmit data
in the same direction.

Fig. 2 is a more detailed block diagram of a prior art node (A,
B, C, D or E) in the network illustrated in Fig. 1. In Fig. 2, a left hand
connection point 5L includes a clock signal line 7L and a data signal line
15 9L. The clock signal line 7L and data signal line 9L are coupled to an
adjacent node (not shown). The clock signal line 7L and data signal line
9L are coupled to bidirectional terminals of a bidirectional bus driver
10L. A clock output terminal and a data signal output terminal from the
bidirectional bus driver 10L are coupled to corresponding input terminals
20 of a receiver 20L. A bidirectional data terminal of the receiver 20L is
coupled to a corresponding data terminal of a memory 30 via a data bus
25. The bidirectional data terminal of the memory 30 is also coupled to
an input terminal of a transmitter 50L via the data bus 25. A clock
output terminal of the transmitter 50L is coupled to a corresponding clock
25 input terminal of the bidirectional bus driver 10L, and a data output
terminal of the transmitter 50L is coupled to a corresponding data input
terminal of the bidirectional bus driver 10L. A right hand connection
point 5R is similarly coupled to the memory 30 via bidirectional bus
driver 10R, receiver 20R and tranmitter 50R, and the data bus 25. A
30 control logic circuit 90 provides a control signal for the left and right
bidirectional bus drivers 10L and 10R, respectively.

The memory 30 is also coupled to node equipment 40. This
node equipment 40 could, for example, be a piece of consumer electronics
equipment, such as a television receiver, VCR, CD player, etc. Although
35 the node equipment 40 is illustrated in Fig. 2 as being coupled to the
memory 30 via a second bidirectional signal line, it is also possible that

3

the memory 30 is coupled to the node equipment 40, and the transmitters (50L and 50R) and the receivers (20L and 20R) via the data bus 25 in a known manner.

The operation of the network of Fig. 1 will be explained with
5   reference to Fig. 2. In Fig. 1 node B desires to transmit data to node D. After the previous message placed on the daisy chain bus has completed transmission, the output drivers of node B begin to drive the daisy chain bus. If an output driver of one or more other nodes simultaneously begin to drive the daisy chain bus, then an arbitration must be performed, in a
10   known manner, to determine which node is to be given use of the daisy chain bus. It is assumed here that node B is the winner of the arbitration. After the arbitration, further processing is performed, also in a known ·
manner, to determine the direction of transmission of the data from node B, through node C, to node D.
15   At this point, the control logic 90 provides a control signal to the right hand connection point of node B which configures the right hand bidirectional bus driver 10R into an output mode, i.e., it is transmitting. The memory 30 supplies data from the node equipment 40 to the transmitter 50R, which serializes the data in a known manner and
20   produces a serial data signal and clock signal, which is supplied to the bidirectional bus driver 10R. The bidirectional bus driver 10R, then supplies these signals to the daisy chain bus of Fig. 1.

Node C is not the recipient for the data produced by node B, and passes the data from it's left hand connection to it's right hand
25   connection unchanged. The left hand connection of node C is configured to receive data from the daisy chain bus. The control logic 90 of node C provides a control signal to the left hand connection of node C which configures the left hand bidirectional bus driver 10L into an input mode, i.e., the bidirectional bus driver 10L of node C is configured to receive
30   data from the daisy chain bus. The data and clock signals received from the daisy chain bus are supplied to the receiver 20L, which decodes the serial data and places that data on the data bus 25. At the same time, the control logic 90 provides a control signal to the right hand connection which configures the right hand bidirectional bus driver 10R into the
35   output mode, i.e., the right hand connection of node C transmits data. The transmitter 50R is configured to serialize the data placed on the data bus

-4

25 by the receiver 20L and generate a corresponding clock signal, and the bidirectional bus driver 10R places the data and clock signals on the daisy chain bus.

Node D is the recipient for the data produced by node B. The
5 left hand connection of node D is configured to receive data from the daisy chain bus. The control logic 90 of node D provides a control signal to the left hand connection which configures the left hand bidirectional bus driver 10L into the input mode, and the bidirectional bus driver 10L of node D receives data from the daisy chain bus. The data and clock
10 signals received from the daisy chain bus are supplied to the receiver 20L, which decodes the serial data and places that data on the data bus 25. The memory 30 stores the data received from the daisy chain bus, and the node equipment 40 accesses and further utilizes this stored data.

This arrangement requires the relatively complicated multi-
15 level sensor conflict detection circuitry described above, and further circuitry to determine data transmission direction, after the arbitration, if any, is complete. A data bus system is desirable, however, which does not require the multiple level sensors to detect a conflict, nor the subsequent processing to determine the required direction for the data
20 ports in each node.

The present invention resides, in part, in recognizing the described problems and, in part, in providing a data bus system that addresses the problems. In accordance with principles of the present invention, a data bus system includes a plurality of nodes coupled
25 together by a daisy chain bus. Each node includes a first and a second bus connection, each having a first and second bidirectional terminal. An arbitration logic is coupled between the first and second bus connection. The node operates in an arbitration mode, during an arbitration time interval, in which the first bidirectional terminal in the first bus
30 connection, and the second bidirectional terminal in the second bus connection are configured to be input terminals, and the second bidirectional terminal in the first bus connection and the first bidirectional terminal in the second bus connection are configured to be output terminals. Then the node operates in a bus access mode in which
35 the first and second bidirectional terminals in the respective first and

5

second bus connections, are both configured to be one of input and output terminals.

In accordance with another aspect of the invention, such a system used the following method to arbitrate among the nodes for access
5 to the daisy chain bus. Each node is preassigned a priority number having a predetermined number of bits. First, the node is placed in an active state. Then, a number of time steps equal in number to the predetermined number of bits in the priority number is performed during an arbitration time interval. For each time step one bit of the
10 priority number is selected. If the selected bit has a superior state, then superior state signals are produced at the output terminals of the first and second bus connections. If the selected bit has an inferior state, and the signals at the input terminals of both the first and second bus connections have inferior states, then inferior state signals are produced
15 at the output terminals of the first and second bus connections Otherwise, the node is placed in a passive state for the remainder of the arbitration time interval, in which signals from the input terminal of the first bus connection are supplied unchanged to the output terminal of the second bus connection, and signals from the input terminal of the second
20 bus connection are supplied to the output terminal of the first bus connection. When the arbitration time interval is over, if the node is in the active state, that node accesses the daisy chain bus.

The invention may be better understood by referring to the enclosed drawing in which:
25   Fig. 1 is a block diagram illustrating a network of nodes arranged on a prior art daisy chain bus;

Fig. 2 is a more detailed block diagram of a node illustrated in the network of nodes of Fig. 1;

Fig. 3 is a more detailed block diagram of a node, which may
30 be arranged in a network of nodes, according to the present invention;

Fig. 4 is an illustration of a network of nodes arranged according to principles of the present invention while conflicting nodes are arbitrating for the use of the bus;

Fig. 5 is an illustration of the network of nodes illustrated in
35 after the arbitration is completed;

6

Fig. 6 is an illustration of the network of nodes illustrated in while data is being transmitted from the selected source node to the destination node; and

Fig. 7 is an illustration of the network of nodes illustrated in
5 Fig. 4 in which a reply is sent from the destination node to the previously selected source node.

Fig. 3 is a more detailed block diagram of a node according to the present invention, which may be arranged in a network of nodes in a similar manner to that illustrated in Fig. 1. Elements similar to those
10 illustrated in Fig. 2 are designated by the same reference numbers, and will not be described in detail below. In Fig. 3, the bidirectional bus drivers 10L and 10R of Fig. 2 are replaced by separately controllable bidirectional bus drivers for the data and clock signal lines, respectively. Referring to the left hand connection 5L, a bidirectional clock signal line
15 bus driver 60L is coupled between clock signal line 7L of the daisy chain bus (of Fig. 1) and the receiver 20L and transmitter 50L. The clock signal line output terminal of the bidirectional clock signal line bus driver 60L is also coupled to a left hand clock signal line input terminal CL of an arbitration logic circuit 80. In a similar manner, a bidirectional data
20 signal line bus driver 70L is also coupled between the data signal line 9L of the daisy chain bus and the receiver 20L and transmitter 50L. The data signal line output terminal of the bidirectional data signal line bus driver 60L is also coupled to a left hand data signal line input terminal DL of an arbitration logic circuit 80. The right hand connection is arranged in
25 a similar manner. A control logic circuit 90' has respective output terminals coupled to corresponding input terminals of the left hand and right hand clock bidirectional clock signal line bus drivers 60L and 60R; and the left hand and right hand bidirectional data signal line bus drivers 70L and 70R.

30   For normal data transfer operations, the left hand clock and data signal line bidirectional bus drivers, 60L and 70L, receive respective control signals from the control logic 90' which configure them to transfer clock and data signals, respectively, in the same direction. I.e. either both are configured to operate as input terminals, or both are configured to
35 operate as input terminals. The right hand clock and data signal line bidirectional bus drivers, 60R and 70R, are similarly configured in

7

response to respective control signals from the control logic circuit 90'. In addition, the respective clock and data signal line bidirectional bus drivers, 60 and 70 L and R, respectively, are coupled to the appropriate one of the transmitters 50 L and R, and receivers 20 L and R, in the

5   manner described above with reference to Fig. 1 and Fig. 2. However, during arbitration operations, the bidirectional clock signal bus driver 60 is controlled separately from the bidirectional data signal bus driver 70, in response to respective signals from the control logic 90'. These operations are better understood by referring to Fig. 4, Fig. 5, Fig. 6 and

10   Fig. 7.

Fig. 4, Fig. 5, Fig. 6 and Fig. 7 are illustrations of a network of nodes according to the present invention, and illustrated in Fig. 3, arranged on a daisy chain bus, and operating in respectively different modes. The network illustrated in these figures is similar to that

15   illustrated in Fig. 1. In Fig. 4, the bus is in an arbitration mode. Various approaches to initiating arbitration are known. For example, an arbitration time interval can be required prior to the start of every data transfer on the daisy chain bus, i.e., whenever any of nodes A, B, C, D and E, in Fig. 4 requires access to the bus. Another approach is to designate a

20   node to be a bus master which controls the initiation of an arbitration time interval. One criterion which may be used to decide when to initiate an arbitration is when the chain bus has been quiescent for a predetermined amount of time. For the purposes of the present invention, it is assumed that before an arbitration according to the

25   present invention occurs, it is initiated using any one of the known techniques.

According to the present invention, each node is preassigned a unique priority number consisting of a predetermined number of bits. When two or more nodes contend for use of the daisy chain bus, the

30   priority numbers for those nodes are compared, in a manner to be described below, and the node with the highest priority, as represented by it's priority number, is granted use of the daisy chain bus.

Referring to Fig. 4, the clock signal line and data signal lines of the daisy chain bus are used for arbitration, and do not carry data or

35   clock signals for transfer of information. The bidirectional clock signal bus drivers 60 in all of the nodes are configured for transferring data in

8

opposite directions from the bidirectional data signal bus drivers 70 in
response to respective control signals from the control logic 90'. For
example, as illustrated in Fig. 4, the clock signal line bus drivers are
configured for transferring signals from the left side of the figure to the
5 right, the data signal line bus drivers are configured for transferring data
from the right side to the left, and the inputs at the end nodes are
coupled to a source of a logic '1' signal. In this illustrated embodiment, a
logic '0' signal indicates a superior state and a logic '1' indicates an
inferior state.

10   An arbitration time interval includes a predetermined
number of time steps, equal to the number of bits in the priority number
assigned to each node. At each time step in the arbitration time interval,
one of the bits of the priority number in each node is tested in a manner
to be described in detail below. In the illustrated embodiment, the bit in
15 the priority number tested in all of the nodes during the first time step of
the arbitration time interval is the most significant bit, the bit tested in
the second time step is the second most significant bit, and so forth. One
skilled in the art will understand, however, that the order in which the
bits are tested is not important so long as the corresponding bit is tested
20 in all the nodes, and all of the bits in the priority numbers are tested at
some time during the arbitration time interval. At the end of the
arbitration time interval, the contending node with the highest priority,
as represented by its priority number, will be granted use of the bus.

          Referring to Fig. 4, during the arbitration time interval, the
25 signal on the clock signal line in the daisy chain bus passes from the left
hand side to the right hand side, and the clock signal line input to the left
most node A is tied to a source of an inferior state (logic '1') signal. In
each of the nodes, A, B, C, D, and E, the left hand clock signal line bus
driver 60L is configured by the control logic circuit 90' to receive a signal
30 from the daisy chain bus which is supplied to the arbitration logic 80.
The arbitration logic 80 generates a signal for the right hand clock signal
line bus driver 60R in a manner to be described below. The right hand
clock signal line bus driver 60R is configured by the control logic circuit
90' to transmit this signal to the daisy chain bus.

35   In a similar manner, the signal on the data signal line in the
daisy chain bus passes from the right hand side to the left hand side, and

9

the data signal line input to the right most node E is tied to a source of an
inferior state (logic '1') signal. In each of the nodes A, B, C, D, and E, the
right hand data signal line bus driver 70R is configured by the control
logic circuit 90' to receive a signal from the daisy chain bus which is
5 supplied to the arbitration logic 80. The arbitration logic 80 generates a
signal for the left hand data signal line bus driver 70L in a manner to be
described below. The left hand data signal line bus driver 70L is
configured by the control logic circuit 90' to transmit this signal to the
daisy chain bus.

10   If a node is not contending for access to the daisy chain bus,
then it remains passive. The signal CL from the left hand clock signal line
bus driver 60L is passed by the arbitration logic 80 unchanged to the
right hand clock signal line bus driver 60R, and the signal DR from the
right hand data signal line bus driver 70R is passed unchanged by the
15 arbitration logic 80 to the left hand data signal line bus driver 70L.

          For each time step in the arbitration time interval, each node
which is contending for access to the daisy chain bus, processes the
signals received from the daisy chain bus and a selected bit in the
priority number, as described above. For example, for the first time step
20 in the arbitration time interval, the first bit of the priority number in
each node (the most significant bit in the illustrated embodiment) is
processed in the respective arbitration logic circuits 80 in each of the
nodes contending for access to the daisy chain bus. If this bit is a
superior state (logic '0') signal, the arbitration logic 80 provides a superior
25 state (logic '0') signal CR to the right hand side clock signal line bus driver
60R, and a superior state (logic '0') signal DL to the left hand side data
signal line bus driver 70L.

          If this bit is an inferior state (logic '1') signal, the arbitration
logic 80 analyzes the clock signal line signal CL from the left hand
30 connection, and the data signal line signal DR from the right hand
connection. If either one of these signals is a superior state (logic '0')
signal, then this node has lost the arbitration, and ceases to arbitrate for
the remainder of the arbitration time interval. This node then becomes
passive, and passes signals received at its daisy chain bus input terminals
35 to the corresponding daisy chain bus output terminals unchanged, as
described above with respect to nodes which are not arbitrating for

10

access to the daisy chain bus. If both of the signals at the daisy chain bus
input terminals are inferior state (logic '1') signals, then this node is still
in contention for access to the daisy chain bus. In this case, the
arbitration logic 80 provides an inferior state (logic '1') signal CR to the
5 right hand side clock signal line bus driver 60R, and an inferior state
(logic '1') signal DL to the left hand side data signal line bus driver 70L.

          At the next time step, the next bit of the priority numbers of
each of the nodes still contending for access to the daisy chain bus are
processed in the same manner described above. For example, during the
10 time step after the first time step of the arbitration time interval during
which the most significant bit of the priority number is considered, the
second most significant bit is processed. This continues until all the time
steps have occurred, all bits in the priority numbers have been processed,
and the arbitration time interval ends.

15   After completion of the arbitration time interval, only one of
the nodes remains active, termed the winning node below, and that node
is granted daisy chain bus access. Fig. 5 is an illustration of the network
of nodes illustrated in Fig. 4 after the arbitration is completed. In Fig. 5,
node B is the winning node of an arbitration time interval. It is
20 transmitting superior state (logic '0') signals from both of its daisy chain
output terminals. All other nodes are in the passive mode. Because the
ends of the bus are coupled to sources of an inferior state (logic '1') signal,
each of the nodes between the winning node B and the end of the bus
sees a superior state (logic '0') signal on the daisy chain bus input
25 terminal on the side of the winning node B, and an inferior state (logic '1')
signal on the other daisy chain bus input terminal. Each node now knows
the relative location of the winning node, that is, the winning node is on
the side which is receiving a superior state (logic '0') signal.

          Because each node knows the relative location of the winning
30 node after arbitration, the logic circuit 90' can configure the bidirectional
bus drivers, 60 L and R, and 70 L and R, to transfer the data from the
winning node without further processing being necessary. Fig. 6 is an
illustration of the network of nodes illustrated in Fig. 4 while data is
being transmitted from the selected source node (node B) to the
35 destination node (node D). As can be seen in Fig. 6, all nodes have
configured their bidirectional bus drivers 60 L and R and 70 L and R to

11

transfer data away from the winning node B. The winning node B transmits its data in both directions simultaneously on the daisy chain bus without regard for the relative location of the desired destination node. In this manner, node B may transfer data to node D, as in Fig. 1.

5   If an immediate response is required from node D to node B, all nodes reverse the direction of their bidirectional bus drivers 60 L and R and 70 L and R, and Node B is configured to receive data from the daisy chain bus. Node D now transmits data in both directions on the bus as shown in Fig. 7, ensuring that node B receives it.

10   In the embodiment illustrated and described, an in-line daisy chain bus system is described. One skilled in the art will understand that a similar arbitration scheme may be equally applicable to a daisy chain ring bus, provided one of the nodes on the ring is designated as the master node. The master node defines the end points of the bus during

15 the arbitration time interval. In addition, in the illustrated embodiment, a superior state signal has been defined as a logic '0' signal and an inferior state signal has been defined as a logic '1' signal. One skilled in the art will also understand that a superior state signal may instead be defined as a logic '1' signal and an inferior state signal may be defined as

20 a logic '0' signal.

12
CLAIMS

1.   In a data bus system, including a plurality of nodes
coupled together by a daisy chain bus, each node comprising:
5   a first and a second bus connection, each comprising a first
and second bidirectional terminal; and
         arbitration logic coupled between the first and second bus
connection; wherein:
         a node operates in an arbitration mode, during an arbitration
10 time interval, in which the first bidirectional terminal in the first bus
connection, and the second bidirectional terminal in the second bus
connection are configured to be input terminals, and the second
bidirectional terminal in the first bus connection and the first
bidirectional terminal in the second bus connection are configured to be
15 output terminals; and
         the node operates in a bus access mode in which the first and
second bidirectional terminals in the respective first and second bus
connections, are both configured to be one of input and output terminals.

20   2.   The system of claim 1 wherein the arbitration logic
further comprises:
         a memory for storing a priority number having a
predetermined number of bits;
         means for placing the node in the arbitration mode;
25   means for placing the node in an active state;
         means for performing the predetermined number of time
steps during the arbitration time interval, and for each step:
              selecting a respective one of the bits in the
              priority number;
30   if the selected bit has a superior state,
              conditioning the output terminals of the first and
              second bus connections to produce superior state signals;
              if the selected bit has an inferior state, and
              signals at the input terminals of both the first
35   and second bus connections are inferior state
              signals, then conditioning the output terminals of

13

the first and second bus connections to produce
inferior state signals; and

otherwise, for the remainder of the
arbitration time interval, placing the node in a

5   passive state in which signals at the input
terminal of the first bus connection are supplied
unchanged to the output terminal of the second
bus connection, and signals at the input terminal
of the second bus connection are supplied

10   unchanged to the output terminal of the first bus
connection; and

means for placing the node in the bus access mode after the ⋅
arbitration time interval, and if the node is in the active state,
conditioning both the first and second bidirectional terminals of both the

15 first and second bus connections to be output terminals.

3.   The system of claim 2 wherein the means for placing the
node in the active state further comprises:

means for determining if the node desires access to the daisy

20 chain bus; and

means for placing the node in the active state if the node
desires access to the daisy chain bus, and placing the node in the passive
state for the arbitration time interval otherwise.

25   4.   The system of claim 2 wherein the means for placing the
node in the bus access mode further comprises means for, if the node is in
the passive state, conditioning the first and second bidirectional terminals
of the bus connection receiving a superior signal to be input terminals,
and the first and second bidirectional terminals of the bus connection

30 receiving an inferior signal to be output terminals.

14

5.   In a data bus system, comprising a plurality of nodes, coupled together by a daisy chain bus, each node having a preassigned priority number having a predetermined number of bits, and comprising
5   a first and a second bus connection, each having an input terminal and an output terminal, a method for each node to arbitrate for access to the daisy chain bus, comprising steps of:

placing the node in an active state;

performing a predetermined number of time steps in an
10 arbitration time interval, and for each time step;

selecting a respective bit of the priority number;

if the selected bit has a superior state, then producing superior state signals at the output
15 terminals of the first and second bus connections;

if the selected bit has an inferior state, and   the signals at the input terminals of both the first and second bus connections have inferior states, then producing inferior state signals at
20 the output terminals of the first and second bus connections; and

otherwise, placing the node in a passive state for the remainder of the arbitration time interval, in which signals from the input terminal   of
25 the first bus connection are supplied unchanged to the output terminal of the second bus connection, and signals from the input terminal of the second bus connection are supplied to the output terminal of the first bus
30 connection; and

if the node is in the active state, accessing the daisy chain bus.

15

6.   The method of claim 5, in which the first and second bus connections in the data bus system each comprise first and second bidirectional terminals, further comprising the steps of:

5   conditioning the first bidirectional terminal in the first bus connection and the second bidirectional terminal in the second bus connection to be the input terminals, and conditioning the second bidirectional terminal in the first bus connection and the first bidirectional terminal in the second bus connection to be the output
10 terminals; wherein

the step of accessing the daisy chain bus comprises the steps of:

                    if the node is in the passive state, then
                    conditioning the bidirectional terminals of the
15   bus connection receiving a superior signal to   both be
                    input terminals, and conditioning the
                    bidirectional terminals of the bus connection   receiving
                    an inferior signal to both be output
                    terminals; and
20   if the node is in the active state, then
                    conditioning both the first and second   bidirectional
                    terminals of both the first and
                    second bus connections to be output terminals.

25   7.   The method of claim 6 wherein the step of accessing the daisy chain bus further comprises the step of: if the node is in the active state and after the conditioning step, sending data to a destination node.

        8.   The method of claim 7 wherein the step of accessing the
30 daisy chain bus further comprises, after the step of sending data to a destination node, the steps of:
                    conditioning both the first and second bidirectional terminals of the both the first and second bus connection to be input terminals; and
   receiving reply data from the destination node.
35

16

9.   The method of claim 5 wherein the step of placing the node in an active state comprises the steps of:

determining if the node desires access to the daisy chain bus; and

5   if the node desires access to the daisy chain bus, placing the node in the active state, otherwise placing the node in the passive state for the arbitration time interval.
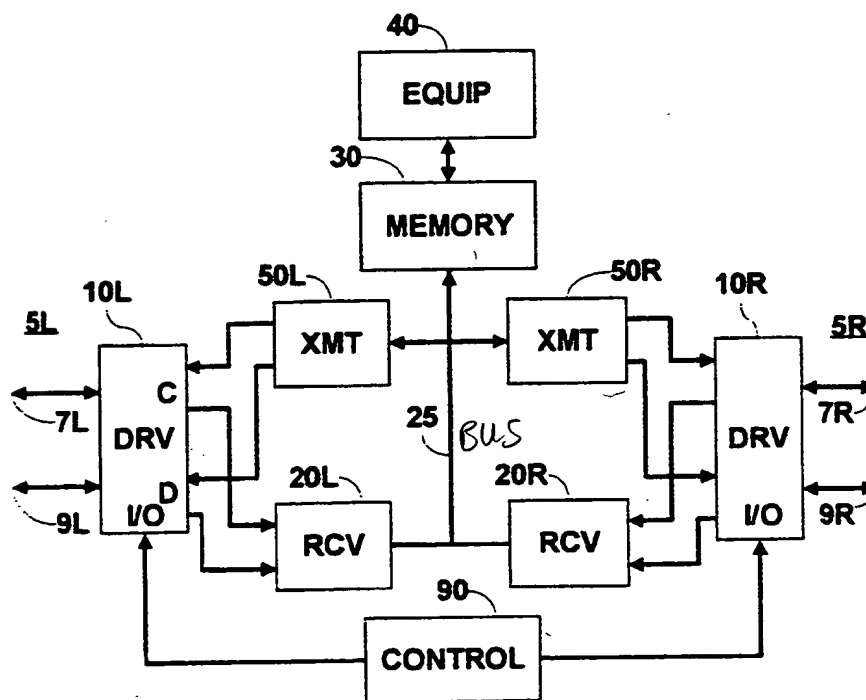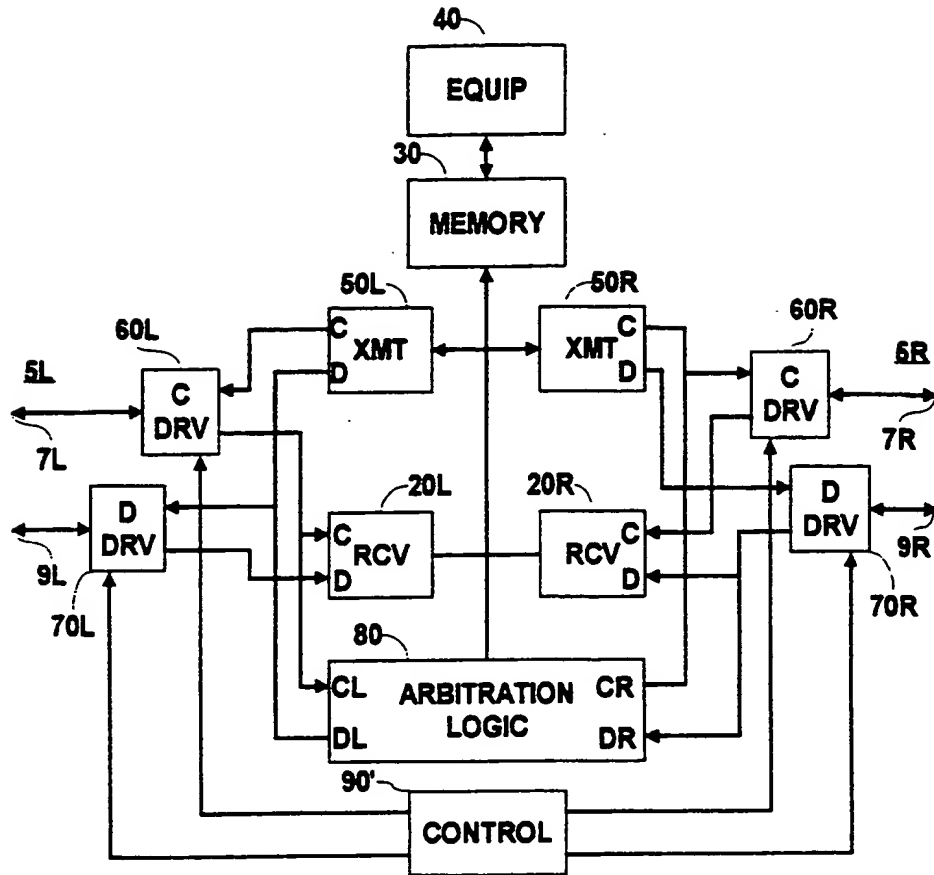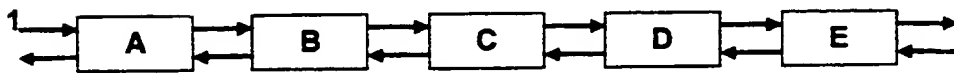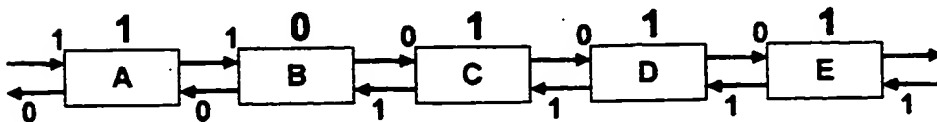
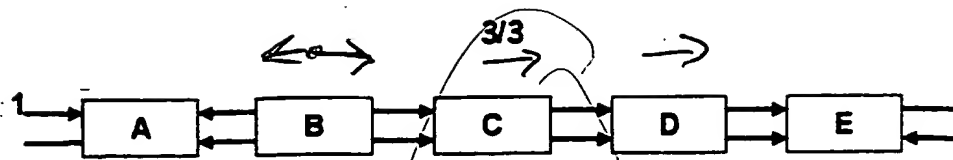**Fig. 1**

Fig. 2

Fig. 3

Fig. 4

Fig. 5

3/3

Fig. 6
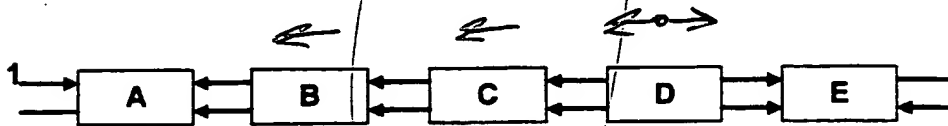
Fig. 7

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6   H04L12/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6   H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category°	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO,A,94 22247 (APPLE COMPUTER) 29 September 1994 see abstract see page 12, line 13 - page 13 see page 22, line 7 - line 18 ---	1-9
A	WO,A,91 17615 (CATERPILLAR INC) 14 November 1991 see page 6, line 20 - page 11, line 6 -----	1-9

☐ Further documents are listed in the continuation of box C. ·   ☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

2 August 1996

Date of mailing of the international search report

22. 08. 96

Name and mailing address of the ISA
    European Patent Office, P.B. 5818 Patentlaan 2
    NL - 2280 HV Rijswijk
    Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
    Fax: (+31-70) 340-3016

Authorized officer

Mikkelsen, C

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
WO-A-9422247	29-09-94	US-A-	5384769	24-01-95
		AU-B-	6405894	11-10-94
		CA-A-	2158155	29-09-94
		EP-A-	0689743	03-01-96
WO-A-9117615	14-11-91	US-A-	5124990	23-06-92
		AU-B-	4174193	16-09-93
		AU-B-	640691	02-09-93
		AU-B-	6352990	27-11-91
		CA-A-	2081102	09-11-91
		DE-D-	69022601	26-10-95
		DE-T-	69022601	09-05-96
		EP-A-	0527734	24-02-93